Chapter 6
Conclusions and Future Work

6.1 Summary and Contributions

In early days the system performance was only considered to be an important factor and hence, the designers were developing the implementations by focusing only on speed and the performance of the system and the concern for power consumption requirements of the system was not given sufficient attention. But because of advancement of device technology, which has doubled the system complexity after almost every 18 – 24 months; and along with the performance, the system power consumption has also raised to considerable level. This increased power requirement has introduced newer challenges in connection with the system power dissipation, thermal parameters and hence the overall system reliability. The power reduction methodologies can be implemented at various abstraction levels of the implementation designing.

This dissertation work has proposed very unique power saving techniques which are implemented at the hardware design level up on the implementation under consideration, in our case, it is five stage pipelined processor (Standard Processor) based on RISC principle and the modification in the pipeline architecture of the standard processor has been done and various proposed dynamic power saving techniques are incorporated in this processor. Then the system is implemented on SPARTEN – 3E FPGA for testing and verification purpose.

As the system is targeted to be implemented on the FPGA the state-of-the-art literature survey has been presented in Chapter 2 which includes various FPGA technologies, internal architectures and also discussed the various dynamic and static power consumption sources of the MOS based systems. It also discusses the mathematical relevance of the power consumption resources.
The dynamic power reduction possibility lies at different abstraction levels and many techniques are available which can be applied at device level, architecture, logical or system architectures level. The detailed survey on existing power reducing techniques is included in Chapter 3. The span of this Ph. D. work is restricted to the application of newly derived energy saving techniques implemented at architecture level i.e. at hardware level.

A standard processor with five pipeline stages is constructed in modular fashion. The formation of subset of instructions is tested and validated through the simulation waveform for number of the programs and correct functionality is recorded. It is estimated and analysed for its power requirement using Xilinx Xpower Estimator and Xpower Analyzer, the reported power consumption is 113 mW. This dissertation work has suggested four unique dynamic power reducing techniques named as Memory Access Stage Removal, Resource Sharing, A novel RAM Addressing Scheme and a Clock Gating arrangement.

By applying memory access stage removal the pipeline structure of the standard processor is modified and made it of four stage pipelined processor. Then the newly formed processor is analyzed for its power requirement which is 110 mW. Hence, the power reduction of 2.65% is achieved compared to that of standard processor. The other technique resource sharing is applied up on the newer processor and analyzed for power consumption which is recorded as 106 mW; means it further reduces the 4 mW (3.63%). The RAM Addressing Scheme and the Clock Gating is applied together on this improved design which consumes the 89 mW only without affecting the performance of the processor. Hence, this strategy again reduces the 17 mW (16%). Here Clock Gating has played a major role in reducing the power consumption and the overall reduction in system power consumption is achieved up to 21%.

6.2 Future Work

The work presented in this thesis provides suggestions to be implemented at hardware level to correct the whole system that strongly impact the power consumption of some complex embedded system and come out with some ideas that efficiently reduces the system power consumption.
However, some interesting points of future research have emerged during the evolution of this work. Many of them are related to the designed approaches, some of them are referenced to their implementation trends in recent era.

On the other hand, the approaches presented in this work have been designed from power optimization view – point. However, the thermal implications of these approaches are needed to be studied and optimized. It is also required to have in-depth study for these approaches with reference to their manufacturing processes, fabrication processes and its actual feasibility. The proposed system can be further optimized by applying many other existing power saving techniques at different abstraction level.

Finally, the concept of low – power is still in very early stages. It still has to understand the complex mechanism that appears in the system behaviour when these newly proposed techniques are applied.

Authors believe that the power management needs multidimensional inputs which are continually expanding with new techniques being developed at every abstraction levels.

6.3 Closing Remark

In summary, we believe that the system level power optimization is an active research area in the years ahead. The techniques proposed in this dissertation provide power reduction on the order of tens of percent, and this is clearly a good beginning. However, further improvements of the same or even with larger magnitude will be needed as processor usage especially in mobile applications increases very rapidly.

The research directions discussed above convinced us to judge that there is considerable space for improvement in the domain of system power consumption.

Yet, it is too early to say that which methodology will help the society to solve the problem of power dissipation. But it is for sure that this work can be taken as base and one can keep developing and adding more and more techniques to the proposed implementation at different levels and can design low – power implementations.