List of Figures

Figure 1.1: Power Reduction Opportunities ................................................................. 3
Figure 2.1: Anti Fuse - Switch ..................................................................................... 16
Figure 2.2: The EPROM Transistor .......................................................................... 16
Figure 2.3: SRAM Cell with (a) Pass – Transistor, (b) Transmission Gate, (c) Multiplexer ......... 18
Figure 2.4: HRL SRAM Cell ....................................................................................... 18
Figure 2.5: A 2- Input LUT ......................................................................................... 19
Figure 2.6: Multiplexer – Based Logic Cell ................................................................. 20
Figure 2.7: Multiplexer and Basic Gates LCELL Proposed by Atmel TM (Courtesy of Atmel TM Co.) ............... 21
Figure 2.8: Actel TM ACT1 Interconnect Architecture (Row – Based) .......................... 22
Figure 2.9: XC4000E/XL/XV Interconnect Architecture (Segmented – Based) (Courtesy of Xilinx TM Corporation) .............................................................. 23
Figure 2.10: XC4000 Series Interconnect Resources (Courtesy of Xilinx TM Co) ................. 23
Figure 2.11: Hierarchical Interconnect (Courtesy of Altera TM Corporation) ................... 24
Figure 2.12: Embedded Memory (a) Block, (b) Distributed Cells ................................. 25
Figure 2.13: Standard CMOS Inverter ........................................................................ 26
Figure 2.14: DC Transfer Characteristics of a CMOS Inverter, (a) Voltage and (b) Current .................... 27
Figure 2.15: Input Voltage and Short – Circuit Current .................................................. 32
Figure 2.16: TTL Input Buffer .................................................................................... 35
Figure 2.17: Tri – State Output Buffer ......................................................................... 36
Figure 3.1: Transistor Reordering .............................................................................. 44
Figure 3.2: Gate restructuring (Figure adapted from the Pennsylvania State University Microsystems Design Laboratory’s tutorial on Low Power Design) ................................................................. 45
Figure 3.3: Low Voltage Differential Signalling ............................................................ 49
Figure 3.4: Bus Segmentation ..................................................................................... 49
Figure 3.5: Two Bit Charge Recovery Bus ................................................................. 50
Figure 3.6: Dead Block Elimination .......................................................................... 54
Figure 3.7: Performance Versus Power ....................................................................... 62
Figure 4.1: Detailed Architecture of 4 – Stage Pipelined Processor Under Consideration ............ 71
Figure 4.2: An ALU Architecture for 4 – Stage CPU ..................................................... 75
Figure 4.3: Formats for Various Instructions ................................................................. 77
Figure 4.4: Detailed Internal Architecture of Instruction Decoder .................................... 81
Figure 4.5: Internal Architecture of Multiplexer ............................................................ 82
Figure 4.6: Diagram of Instruction Decoder with all relevant Signals ............................... 83
Figure 4.7: Main Features of Multiplier Block ............................................................... 85
Figure 4.8: Pin Diagram of MULT18X18SIO ................................................................. 86
Figure 4.9: Four possible Configures for the B_INPUT Attribute and BREG Attribute ............................................... 87
Figure 4.10: Xilinx SPARTAN – 3E Clock Distribution Network (Courtesy of Xilinx™ Co.) ........................................ 88
Figure 4.11: Internal Element of 2 – to -1 Multiplexer (Courtesy of Xilinx™ Co.) ................................................... 89
Figure 4.12: Quadrant – Based Clock Routing (Courtesy of Xilinx™ Co.) .............................................................. 90
Figure 4.13: Data Dependency and Data Forwarding ................................................................................................. 94
Figure 4.14: External Interface ................................................................................................................................. 94
Figure 4.15: FPGA Design Flow ............................................................................................................................. 95
Figure 4.16: Summary of Estimated Power Distribution Report ............................................................................. 97
Figure 4.17: Graphical Representation of Estimated Power Requirements for Internal Modules and Effect of Various Parameters on Power Consumption ................................................................. 98
Figure 5.1: Detailed Architecture of 5 – Stage Pipelined Conventional CPU ................................................................. 102
Figure 5.2: Summary of Power Consumption Report for 5 – Stage Pipeline CPU .................................................... 103
Figure 5.3: Instruction Fetch for 5 - Stage CPU ........................................................................................................ 104
Figure 5.4: Instruction Decode for 5 – Stage CPU ...................................................................................................... 105
Figure 5.5: RAM Address for 5 – stage CPU ........................................................................................................... 106
Figure 5.6: Instruction Execute for 5 - Stage CPU .................................................................................................... 107
Figure 5.7: Write Back Stage for 5 – Stage CPU ........................................................................................................ 108
Figure 5.8: Summary of Power Consumption Report for 4 – Stage Pipeline CPU (After Implementation of Memory Access Stage Removal) .............................................................................................. 111
Figure 5.9: Instruction Fetch for 4 – Stage CPU ....................................................................................................... 112
Figure 5.10: Instruction Decode and Operand Fetch for 4 – Stage CPU ................................................................. 113
Figure 5.11: Instruction Execute for 4 – Stage CPU ................................................................................................. 114
Figure 5.12: Write Back for 4 – Stage CPU .............................................................................................................. 115
Figure 5.13: MUX for Resource Optimization ......................................................................................................... 117
Figure 5.14: MUX with Opcode as Selection Logic ................................................................................................. 118
Figure 5.15: Summary of Power Consumption Report for 4 – Stage Pipeline CPU (After Implementation of Resource Sharing Strategy) ........................................................................................................ 119
Figure 5.16: RAM Address Multiplexer ................................................................................................................ 120
Figure 5.17: Clock – Enabled Global Buffer Resource ............................................................................................... 121
Figure 5.18: Gated Clock – Not Preferable ............................................................................................................... 121
Figure 5.19: Clock Enable – Efficient way of Gating a Clock Signal ........................................................................ 121
Figure 5.20: Summary of Power Consumption Report for 4 – Stage Pipeline CPU (After Implementation of RAM Addressing Scheme and Clock Gating along with earlier Techniques) ............................................................................................. 125
Figure 5.21: Simulated Waveforms for Clk_gating Signal Varification for ALU Related Instructions .................... 126
Figure 5.22: Simulated Waveforms for Clk_gating Signal Verification during RAM Access Instructions ............ 127
Figure 5.23: Verification of Instruction Fetch for 4 – Stage CPU ............................................................................. 129
Figure 5.24: Verification of Instruction Decode and Operand Fetch for 4 – Stage CPU ............................................. 130
Figure 5.25: Verification of Instruction Execute for 4 – Stage CPU ........................................................................... 131